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10/567,171	02/03/2006	Martin J. Edwards	GB030133US1	9639

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EXAMINER	
MORRIS, JOHN J	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
03/05/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,171	EDWARDS ET AL.	
	Examiner	Art Unit	
	John Morris	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claim 1, the applicant argues that Miyake's capacitors 2154 and 2155 are not voltage dependent. The examiner respectfully disagrees. The applicant agrees that Miyake's capacitors 2154 and 2155 are voltage-controllable, but argues that they are not used as voltage-dependent capacitors. However, if a capacitor is voltage controlled then it's inherent that its capacitance is dependent on the voltage. The voltage could turn on or off the capacitor, thereby changing the capacitance, which makes this capacitance voltage dependent as well. Therefore these capacitors are voltage dependent. The combination of Miyake with Tomooka would affect the image quality by allowing a high load driving capability as well as a shorter rise time, therefore improving the image quality.

The applicant argues that Tomooka refers to the fixed-capacitance capacitor as the pixel capacitor and one would be reluctant to apply varying control voltages to the pixel-element to change its capacitance. However, Tomooka already has one variable capacitor (Tomooka, figure 5, item 7), therefore one would conclude that the addition of another variable capacitor would work. The combination of Tomooka and Miyake would allow for a high load driving capability as well as a shorter rise time and would provide the structure of two voltage-dependent capacitors, therefore given the functionality claimed.

Therefore, the examiner respectfully disagrees with the applicant and the rejection stands.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 19-21, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*) in view of Kobayashi et al. (US Pat# 4432610/ *or "Kobayashi" hereinafter*) and Suzuki et al. (US Pat# 4621260/ *or "Suzuki" hereinafter*).

For **claim 1,** Tomooka teaches an amplification circuit (Tomooka, column 2, lines 36-38) comprising: an input to which an input voltage is provided (Tomooka, figure 5, item 4), a capacitor arrangement (Tomooka, figure 5, items 6 and 7), and a switching arrangement (Tomooka, figure 5), wherein the capacitor arrangement includes a first capacitor that is configured as a voltage-dependent capacitor having a first voltage-dependent capacitance (Tomooka, figure 5, item 7). Tomooka teaches the circuit is operable in two modes, a first mode in which the input voltage is provided to an input terminal of at least the first capacitor (Tomooka, column 4, lines 24-39). Tomooka teaches the switching arrangement is configured to receive a first gain-control signal that is arranged to change the capacitance of the first capacitor (Tomooka, column 2, lines 48-63). Tomooka does not teach a second voltage-dependent capacitor; however, in the

same field of endeavor, Kobayashi teaches a second voltage-dependent capacitor having a second voltage-dependent capacitance (Kobayashi, figure 7, items 80 and 82). Kobayashi teaches a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors (Kobayashi, column 6 line 62 - column 7 line 33). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Tomooka with Kobayashi because the addition would allow for a higher resolution at less cost and with a simple construction. Tomooka and Kobayashi do not teach a second gain control signal; however, in the same field of endeavor, Suzuki teaches two capacitors each with their own control signal (Suzuki, figure 3, items 24 and 28). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tomooka and Kobayashi with Suzuki because this would allow control of each capacitor separately which would improve the image quality.

For **claim 2,** Tomooka teaches a switching arrangement includes an input switch for selectively coupling the input voltages to the capacitor arrangement, wherein the first mode the input switch couples the input voltage to the capacitor arrangement, and in the second mode the input switch isolates the input voltage from the capacitor arrangement (Tomooka, column 4, lines 39-50).

For **claim 3,** Tomooka teaches at least one of the first and second gain-control signals change a voltage on a gain-control terminal of the first and/or second capacitor (Tomooka, column 2, lines 50-63)

For **claim 4,** Tomooka teaches the change in voltage is on the gain-control terminal of the first capacitor and results in a reduction in the capacitance of the first capacitor (Tomooka, column 4, line 45-48).

For **claim 5,** Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Kobayashi teaches a circuit which uses two voltage dependent capacitors (Kobayashi, figure 7, items 80 and 82). Kobayashi also teaches a voltage on the gain-control terminal of each of the first and second capacitors is changed (Kobayashi, column 7, lines 1-33). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Tomooka with Kobayashi because the addition would allow for a higher resolution at less cost and with a simple construction.

For **claim 6,** Tomooka teaches that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Kobayashi teaches a circuit which uses two voltage dependent capacitors (Kobayashi, figure 7, items 80 and 82). Kobayashi also teaches a voltage on the gain-control terminal of each of the first and second capacitors is changed (Kobayashi, column 7, lines 1-33). Therefore it would have been obvious that a change

in voltage on the gain-control terminal of the second capacitor would also result in a reduction in capacitance.

For **claim 7,** Tomooka teaches that the voltage across the first capacitor can change to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Kobayashi teaches a circuit which uses two voltage dependent capacitors (Kobayashi, figure 7, items 80 and 82). Kobayashi also teaches a voltage on the gain-control terminal of each of the first and second capacitors is changed (Kobayashi, column 7, lines 1-33). Kobayashi teaches the voltage on the gain-control terminal of the first capacitor is increased and the voltage on the gain-control terminal of the second capacitor is decreased (Kobayashi, column 7, lines 1-33).

For **Claim 8,** Tomooka teaches that the voltage across the first capacitor can change to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Kobayashi teaches a circuit which uses two voltage dependent capacitors (Kobayashi, figure 7, items 80 and 82). Kobayashi also teaches a voltage on the gain-control terminal of each of the first and second capacitors is changed (Kobayashi, column 7, lines 1-33). Kobayashi teaches the voltage on the gain-control terminal of the first capacitor is increased and the voltage on the gain-control

terminal of the second capacitor is decreased (Kobayashi, column 3 lines 34-56; column 7, lines 1-33).

For **claim 9,** Tomooka and Kobayashi do not teach the gain-control terminal of the first capacitor controlling the input switch; however, in the same field of endeavor, Suzuki teaches the input switch is controlled by the voltage on the gain-control terminal of the first capacitor (Suzuki, figure 3, item 24). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tomooka and Kobayashi with Suzuki because this would allow control of each capacitor separately which would improve the image quality.

For **Claim 10** Suzuki teaches the input switch includes a first transistor (Suzuki, figure 3, item 20) with a gate connected to the gain-control terminal of the first capacitor (Suzuki, figure 3).

For **claim 19,** Tomooka teaches a circuit wherein the voltage dependent capacitor comprises a transistor with source and drain connected together. Tomooka and Kobayashi do not teach the gate terminal connected to the capacitor; however, in the same field of endeavor, Suzuki teaches one of the input terminals and gain-control terminal is defined by the gate and another of the input and gain-control terminal is defined by the connected source and drain (Suzuki, figure 3, items 20 and 24). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify

Tomooka and Kobayashi with Suzuki because this would allow control of each capacitor separately which would improve the image quality

For **claim 20,** Tomooka does not state that the transistor is a thin film MOS transistor; however, the examiner takes official notice that it was well known in the art for the transistor to be a thin film MOS transistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tomooka because the use of a thin film transistor would decrease the weight of the device.

For **claim 21**, Tomooka teaches an active matrix device comprising an array of device elements and circuitry for generating control signals for controlling the device elements, further comprising a circuit for increasing a voltage level of the control signals before supply to the device elements (Tomooka, abstract). Tomooka teaches an LCD with driving circuitry, which is well known to be an active matrix device which comprises an array of device elements.

For **claim 23**, Tomooka teaches an amplification circuit (Tomooka, column 2, lines 36-38) comprising: an input to which an input voltage is provided (Tomooka, figure 5, item 4), a capacitor arrangement (Tomooka, figure 5, items 6 and 7), and a switching arrangement (Tomooka, figure 5), wherein the capacitor arrangement includes a first capacitor that is configured as a voltage-dependent capacitor having a first voltage-dependent capacitance (Tomooka, figure 5, item 7). Tomooka teaches the circuit is

operable in two modes, a first mode in which the input voltage is provided to an input terminal of at least the first capacitor (Tomooka, column 4, lines 24-39). Tomooka teaches the switching arrangement is configured to receive a first gain-control signal that is arranged to change the capacitance of the first capacitor (Tomooka, column 2, lines 48-63). Tomooka teaches an active matrix device comprising an array of pixels and circuitry for generating control signals for controlling the device elements, further comprising a circuit for increasing the voltage level of the control signals before supply to the device elements (Tomooka, abstract). Tomooka teaches an LCD with driving circuitry, which is well known to be an active matrix device which comprises an array of pixels. Tomooka does not teach a second voltage-dependent capacitor; however, in the same field of endeavor, Kobayashi teaches a second voltage-dependent capacitor having a second voltage-dependent capacitance (Kobayashi, figure 7, items 80 and 82). Kobayashi teaches a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors (Kobayashi, column 6 line 62 - column 7 line 33). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Tomooka with Kobayashi because the addition would allow for a higher resolution at less cost and with a simple construction. Tomooka and Kobayashi do not teach a second gain control signal; however, in the same field of endeavor, Suzuki teaches two capacitors each with their own control signal (Suzuki, figure 3, items 24 and 28). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tomooka and Kobayashi with Suzuki because this would allow control of each capacitor separately which would improve the image quality.

For **claim 24,** Tomooka teaches storing a display pixel voltage on a storage capacitor, providing a voltage to the display pixel in dependence on the stored display pixel voltage, wherein the writing circuitry comprises the control transistor, the gate voltage of the control transistor being provided by the storage capacitor arrangement, and wherein the storage capacitor arrangement comprises the capacitor arrangement of the amplification circuit (Tomooka, column 4 line 40 - column 5 line 35, figure 5).

Claim 25 is rejected upon the same grounds as claim 21.

For **claim 26**, Tomooka teaches the device elements comprise memory cells, image sensing pixels, or display pixels (Tomooka, abstract).

Claim 27 is rejected upon the same grounds as claim 1.

3. Claims 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*) in view of Kobayashi et al. (US Pat# 4432610/ *or "Kobayashi" hereinafter*), Suzuki et al. (US Pat# 4621260/ *or "Suzuki" hereinafter*), and Miyake et al. (US Pat# 6788108 B2/ *or "Miyake" hereinafter*).

For **claim 11,** Tomooka teaches that the voltage across the first capacitor can change to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 -

column 5 line 3). Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Kobayashi teaches a circuit which uses two voltage dependent capacitors (Kobayashi, figure 7, items 80 and 82). Kobayashi teaches the voltage on the grain-control terminal of the second capacitor is changed (Kobayashi, column 7, lines 1-33). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Tomooka with Kobayashi because the addition would allow for a higher resolution at less cost and with a simple construction. Tomooka and Kobayashi does not teach two transistors in parallel; however, in the same field of endeavor, Miyake teaches two transistors in parallel with each other with the gate of the second transistor connected to the one terminal of the second capacitor (Miyake, figure 21, item 2155 or 2154). It would have been obvious to one of ordinary skill in the art to modify Tomooka and Kobayashi with Miyake because the addition would regulate current flow with the capacitor.

For **claim 12,** Tomooka does not teach input terminals corresponding to the gain-control terminal of each of the first and second capacitor; however, in the same field of endeavor, Kobayashi teaches the input terminal corresponds to the gain-control terminal of each of the first and second capacitors (Kobayshi, figure 7, items 80 and 82). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Tomooka with Kobayashi because the addition would allow for a higher resolution at less cost and with a simple construction. Kobayashi does not teach a switching arrangement with multiple switches; however in the same field of endeavor,

Miyake teaches using multiple switches (Miyake, figure 21). Miyake teaches switches coupling reference, control, and input voltage to the terminals of the first and second capacitor (Miyake, figure 21 and figure 6c). It would have been obvious to one of ordinary skill in the art to modify Tomooka and Kobayashi with Miyake because both are semiconductor devices that can be used with LCD's and the addition of Miyake would allow a high load driving capability as well as a short rise time.

For **claim 13,** Miyake teaches the first switch and input switch closed so that a voltage across the capacitors is dependent on the input voltage (Miyake, figure 21 and 6c) and where the second switches are closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors (Miyake, figure 21 and 6c).

For **claim 14,** Miyake teaches capacitors comprising thin film transistors (Miyake, column 25, lines 3-12). It is obvious that thin film transistors may be n-type MOS devices.

Claim 15 is rejected upon the same grounds as claim 14.

For **claim 16,** Tomooka, Kobayashi, and Suzuki do not teach an input connected to the input terminal of the first and second capacitors and respective gain-control voltages are coupled to the gain-control terminals of the first and second capacitors through respective control switches; however, in the same field of endeavor, Miyake

teaches an input connected to the input terminal of the first and second capacitors and respective gain-control voltages are coupled to the gain-control terminals of the first and second capacitors through respective control switches (Miyake, figure 6c, items 653 and 654). It would have been obvious to one of ordinary skill in the art to modify Tomooka, Kobayashi, and Suzuki with Miyake because both are semiconductor devices that can be used with LCD's and the addition of Miyake would allow a high load driving capability as well as a short rise time.

For **claim 17,** Tomooka, Kobayashi, Suzuki, and Miyake do not teach a shorting switch; however the examiner takes official notice that a shorting switch is well known in the art at the time of the invention. Therefore, it would have been obvious to add one between the terminals of the first and second capacitors, since such a modification only requires a mere addition of a well known component.

For **claim 18,** Miyake teaches the first switch and input switch closed so that a voltage across the capacitors is dependent on the input voltage (Miyake, figure 21 and 6c) and where the second switches are closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors(Miyake, figure 21 and 6c). Miyake does not teach a shorting switch; however the examiner takes official notice that a shorting switch is well known in the art at the time of the invention. Therefore, it would have been obvious to add one between the terminals of the first and second capacitors, since such a modification only requires a mere addition of a well known component.

4. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*) in view of Kobayashi et al. (US Pat# 4432610/ *or "Kobayashi" hereinafter*), Suzuki et al. (US Pat# 4621260/ *or "Suzuki" hereinafter*), and Abe (US Pat# 5694369).

For **claim 22**, Tomooka does not teach a latch circuit; however, in the same field of endeavor, Abe teaches an amplification circuit with an output data latch circuit (Abe, figure 1, items 6 and 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomooka with Abe because both are semiconductor devices with amplification circuits and the addition of an output data latch circuit can improve stability.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sano (US Pub# 20050018503 A1) discloses an amplifier circuit; Sano et al. (US Pub# 20050017929 A1) disclose a pixel circuit and display device; Marr (US Pat# 4021788) discloses a capacitor memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morris whose telephone number is (571)270-7171. The examiner can normally be reached on Monday-Friday, 7am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amr Awad/

Supervisory Patent Examiner, Art Unit 2629